

CLAIMS

What is claimed is:

1. A method comprising:
 - 5 receiving an input voltage for a digital power rail of a display;
regulating the input voltage to a start-up voltage during a start-up period; and
regulating the input voltage to a steady-state voltage after the start-up period,
said steady-state voltage being lower than the start-up voltage.
- 10 2. The method of claim 1 wherein the digital power rail of the display powers at least one of a data driver and a panel controller.
3. The method of claim 1 wherein the start-up voltage is substantially equal to the input voltage.
- 15 4. The method of claim 1 wherein regulating the input voltage to the start-up voltage comprises:
 - passing the input voltage during the start-up period.
- 20 5. The method of claim 1 wherein regulating the input voltage to the steady-state voltage comprises:
 - linearly biasing the input voltage down to the steady-state voltage after a capacitance-induced delay of at least the start-up time.
- 25 6. The method of claim 1 wherein regulating the input voltage to the steady-state voltage comprises:
 - pulse width modulating the input voltage down to the steady-state voltage.

7. An apparatus comprising:
a digital input power rail to receive an input voltage for a display;
a voltage regulator to regulate the input voltage to a start-up voltage during a start-up period, and to regulate the input voltage to a steady-state voltage after the start-up period, said steady-state voltage being lower than the start-up voltage.
8. The apparatus of claim 7 wherein the voltage regulator comprises a pulse width modulator.
9. The apparatus of claim 8 wherein, to regulate the input voltage to the start-up voltage, the pulse width modulator switches the input voltage at a first duty ratio, and, to regulate the input voltage to the steady-state voltage, the pulse width modulator switches the input voltage at a second duty ratio.
10. The apparatus of claim 9 wherein the first duty ratio is 1.
11. The apparatus of claim 9 wherein the second duty ratio is 2.5/3.3.
12. The apparatus of claim 7 wherein the voltage regulator comprises a linear voltage regulator.
13. The apparatus of claim 12 wherein the linear voltage regulator comprises:
a regulating component coupled between a first node and a second node, said first node comprising the digital input power rail, said second node comprising an output power rail;
a first resistive element coupled between the first node and a third node;
a bandgap reference element coupled between a ground node and the third node;
an operational amplifier having an inverting input coupled to the third node, a non-inverting input coupled to a fourth node, and an output coupled to a fifth node;

a second resistive element coupled between the fourth node and the ground node;

a third resistive element coupled between the second node and the fourth node;

5 a first capacitive element coupled between the fourth node and the ground node; and

a second capacitive element coupled between the second node and the ground node.

10 14. The apparatus of claim 13 wherein the regulating component comprises a pass-element transistor.

15 15. The apparatus of claim 14 wherein the pass-element transistor comprises a p-channel metal oxide semiconductor field effect transistor (MOSFET).

16. The apparatus of claim 13 wherein the regulating component is to provide isolation between the first and second nodes.

20 17. The apparatus of claim 13 wherein the bandgap reference element comprises a Zener diode.

25 18. The apparatus of claim 13 wherein the input voltage is 3.3 volts, the steady-state voltage is 2.5 volts, and the bandgap reference element provides a reference voltage of 1.225 volts.

19. The apparatus of claim 13 wherein the first capacitive element provides the start-up period.

20. A machine readable medium having stored thereon machine executable instructions, the execution of which implement a method comprising:

- receiving an input voltage for a digital power rail of a display;
- regulating the input voltage to a start-up voltage during a start-up period; and
- 5 regulating the input voltage to a steady-state voltage after the start-up period, said steady-state voltage being lower than the start-up voltage.

21 The machine readable medium of claim 20 wherein regulating the input voltage to the start-up voltage comprises:

- 10 passing the input voltage during the start-up period.

22. The machine readable medium of claim 20 wherein regulating the input voltage to the steady-state voltage comprises:

- linearly biasing the input voltage down to the steady-state voltage after a
- 15 capacitance-induced delay of at least the start-up time.

23. The machine readable medium of claim 20 wherein regulating the input voltage to the steady-state voltage comprises:

- pulse width modulating the input voltage down to the steady-state voltage.
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24. A system comprising:

- a liquid crystal display (LCD); and
- a power supply coupled to the LCD, said power supply comprising:
 - 25 a digital input power rail to receive an input voltage for the LCD;
 - a voltage regulator to regulate the input voltage to a start-up voltage during a start-up period, and to regulate the input voltage to a steady-state voltage after the start-up period, said steady-state voltage being lower than the start-up voltage.

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25. The system of claim 24 wherein the voltage regulator comprises a pulse width modulator.

26. The system of claim 25 wherein, to regulate the input voltage to the start-up
5 voltage, the pulse width modulator switches the input voltage at a first duty ratio, and, to regulate the input voltage to the steady-state voltage, the pulse width modulator switches the input voltage at a second duty ratio.

27. The system of claim 24 wherein the voltage regulator comprises a linear voltage
10 regulator.

28. The system of claim 27 wherein the linear voltage regulator comprises:

a regulating component coupled between a first node and a second node,
said first node comprising the digital input power rail, said second node comprising
15 an output power rail;

a first resistive element coupled between the first node and a third node;
a bandgap reference element coupled between a ground node and the third
node;

an operational amplifier having an inverting input coupled to the third node, a
20 non-inverting input coupled to a fourth node, and an output coupled to a fifth node;

a second resistive element coupled between the fourth node and the ground
node;

a third resistive element coupled between the second node and the fourth
node;

25 a first capacitive element coupled between the fourth node and the ground
node; and

a second capacitive element coupled between the second node and the
ground node.